FILM DEPOSITION TO ENHANCE SEALING YIELD OF MICROCAP WAFER-LEVEL PACKAGE WITH VIAS

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FIELD OF INVENTION

[0001] This invention relates to a wafer-level hermetic package for a micro device.

DESCRIPTION OF RELATED ART

[0002] A micro-size cap ("microcap") wafer-level package is formed by bonding a cap wafer to a device wafer. The bonding areas are seal rings formed around each die and vias for receiving via contacts or plugs. Due to leaks from defects or contamination in the bonding areas, a packaged device may fail quality and reliability tests where it is exposed to high temperature and humidity. Thus, what is needed is a method to enhance the seal to increase the final product yield.

SUMMARY

[0003] In one embodiment of the invention, a method for forming a wafer package includes forming a die structure, wherein the die structure includes a first wafer, a device mounted on the first wafer, a second wafer mounted atop the first wafer with a first seal ring around the device and a second seal ring around a via contact. The method further includes forming a trench in the second wafer around the first seal ring, filling the trench and the via contact with a sealing agent, patterning a topside of the second wafer to remove the excessive sealing agent and to expose a contact pad of the via contact, and singulating a die around the first seal ring.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Fig. 1 is a flowchart of a method for forming a microcap wafer-level package in one embodiment of the invention.

[0005] Figs. 2A, 2B, 2C, 3, 4, 5, and 6 illustrate cross-sections of the structures formed by the method of Fig. 1 in one embodiment of the invention.

[0006] Fig. 7 illustrates a top view of a structure formed by the method of Fig. 1 in one embodiment of the invention.

[0007] Figs. 8 and 9 illustrate cross-sections of the structures formed by the method of Fig. 1 in another embodiment of the invention.

DETAILED DESCRIPTION

[0008] Fig. 1 is a flow chart of a method 100 for forming a micro-size cap ("microcap") wafer-level package in one embodiment of the invention. In step 101, a base wafer 202 is formed as shown in Fig. 2A. Base wafer 202 includes a device 204 that needs to be hermetically sealed. Base wafer 202 is typically silicon. Device 204 may be an active circuit, a passive sensor, a MEMS (micro electromechanical system) device, or another similar component. A metal layer is deposited on base wafer 202 and patterned with a photoresist layer to form bonding/contact pads 206A and 206B where required. Bonding pads 206 are typically gold. Device 204 can be connected to pads 206B by bond wires or by metal interconnects in base wafer 202.

[0009] In step 102, a microcap wafer 208 is formed as shown in Fig. 2B. A metal layer is deposited on microcap wafer 208 and patterned with a photoresist layer to form bonding pads 207A and 207B where required. The photoresist layer is then used as a mask to etch silicon gaskets 210A and 210B. Gaskets 210A form a perimeter seal ring 211A (Fig. 7) around device 204 while gaskets 210B form via seal rings 211B (Fig. 7) around locations where vias are to be formed. Gaskets 210A and 210B may include a treaded surface and bonding pads 207A and 207B are typically gold. Another photoresist layer is applied and patterned so vias 212 can be etched where via contacts and plugs are to be formed. In an alternative embodiment described later, vias 212 are etched after microcap wafer 208 is bonded to base wafer 202.

[0010] In step 103, base wafer 202 and microcap wafer 208 are aligned and bonded to form a microcap die structure 200 as shown in Fig. 2C. In one embodiment, the wafers are bonded by being compressed together until a cold weld bond forms between pads 206A and 207A, and pads 206B and 207B. Typical bonding conditions for such an embodiment may be

compressing the wafers together between 60 to 120 megapascal at temperatures ranging from 320 to 400°C for 2 minutes to 1 hour. In other embodiments, the wafers might be bonded together by a solder joint, by adhesive, or by glass. In subsequent figures after the bonding, each pair of corresponding pads is shown as one integrated pad.

[0011] Microcap wafer 208 is then thinned to expose vias 212 and provide access to contact pads 206B on base wafer 202. Vias 212 can be optionally widened by an isotropic plasma etch. As the front of via 212 is exposed to more etchant and is etched more rapidly than the back, a sloped via 212 that is wider at the front and narrower at the back is formed. A seed metallization layer is deposited on microcap wafer 208 and sidewalls of vias 212 and patterned with a photoresist layer so via contacts 214 can be formed by electroplating. Via contacts 214 are typically gold. As via contacts 214 are formed by electroplating, they define cavities 215 that may be vulnerable to moisture.

[0012] In step 104, trenches 220 on microcap wafer 208 are formed around gaskets 210A/perimeter seal rings 211A as shown in Figs. 3 and 7. In one embodiment, DRIE (deep reactive ion etching) is used to form trenches 220. Alternatively, a saw can be used to form trenches 220.

[0013] In step 106, trenches 220 and via contacts 214 are partially or fully filled with a sealing agent 230 as shown in Fig. 4. Sealing agent 230 is a coating that inhibits moisture from entering volumes 232. Examples of sealing agent 230 include photoresist, polyimide, B-staged bisbenzocyclobutene (BCB), other polymers, spin-on-glass, glass, Pyrex® (from Corning of New York), oxide, nitride, or metals. Spin-on-glasses can be spun onto microcap wafer 208 to fill trenches 220 and via contacts 214. Glasses and other dielectric materials can fill trenches 220 and via contacts 214 by sol-gel processes. Screen printing of polymers such as epoxy, photoresist, polyimide, and BCB can also be used for filling. Pyrex, oxide, nitrides, and other dielectrics can be coated on trenches 220 and via contacts 214 by evaporation, sputtering, or vapor deposition. Metals might be deposited by evaporation, sputtering, electroplating or electroless plating. Alternatively, a polymer can be used to fill via contacts 214 and trenches 220 and then contact pads 214A can be coated with a dielectric or metal thin film 234 (Fig. 5) above filing agent 230 as an additional barrier against moisture. Polymers can fill via contacts 214 and trenches 220 by spin-coating, screen printing, or injection. Film 234 can be one or multiple layers of gold, titanium, aluminum, tungsten,

titanium tungsten, chromium, nickel, copper, palladium, platinum or an alloy of any preceding metal.

[0014] In step 108, the top surface of microcap wafer 208 is patterned to remove excessive sealing agent 230 and to expose contact pads 214A of via contacts 214 as shown in Fig. 5. In one embodiment, the top surface is wet etched to remove sealing agent 230. Alternatively, the top surface can be dry etched to remove sealing agent 230. In another embodiment, the top surface is polished or chemically-mechanically polished to remove excess sealing agent 230.

[0015] In step 110, a die 240 is singulated from structure 200 along trenches 220 as shown in Fig. 6. In one embodiment, die 240 is singulated with a saw. Alternatively, die 240 can be singualted with a scribe and break tool. As can be seen, sealing agent 230 provides an additional seal around gaskets 210A/perimeter seal rings 211A and an additional seal within via contacts 214 to protect die 240 against moisture and containments.

[0016] In an alternative embodiment shown in Figs. 8 and 9, microcap wafer 208 is etched to form vias 212 after microcap wafer 208 is bonded to base wafer 202. Vias 212 can then be plated and filled as described above.

[0017] Various other adaptations and combinations of features of the embodiments disclosed are within the scope of the invention. Numerous embodiments are encompassed by the following claims.